IN THE SPECIFICATION

Please amend the paragraph beginning at page 1, line 5 as follows:

This application is a Divisional of U.S. Application No. 10/117,041, filed April 5, 2002, now U.S. Patent No. 7,105,914, which is a Divisional of U.S. Application No. 09/484,002, filed January 18, 2000, now U.S. Patent No. 6,376,370, both of which are incorporated herein by reference.

Please delete the paragraphs beginning on page 5, line 15, starting with and including the heading, Summary of the Invention, through page 6, line 7, before the heading Brief Description of the Drawings.

Please insert the following paragraphs beginning on page 8, line 4 before the paragraph beginning on page 8, line 5:

The structures and methods of the present invention include a diffusion barrier and a seed layer in an integrated circuit both formed using a low energy ion implantation followed by a selective deposition of metal lines for the integrated circuit. According to the teachings of the present invention, the selective deposition of the metal lines avoids the need for multiple chemical mechanical planarization (CMP) steps. The low energy ion implantation of the present invention allows for the distinct placement of both the diffusion barrier and the seed layer. A residual resist can be used to remove the diffusion barrier and the seed layer from unwanted areas on a wafer surface.

In particular one illustrative embodiment of the present invention includes a method of making a diffusion barrier and a seed layer in an integrated circuit. The method includes patterning an insulator material to define a number of trenches in the insulator layer opening to a number of first level vias in a planarized surface. A barrier/adhesion layer is deposited in the number of trenches using a low energy ion implantation, e.g. a 100 to 800 electron volt (eV) ion implantation. A seed layer is deposited on the barrier/adhesion layer in the number of trenches also using the low energy ion implantation. This novel methodology further accommodates the formation of aluminum, copper, gold, and/or silver metal interconnects.